Thermal Stress Analysis of Medium-Voltage Converters for Smart Transformers

Andresen, Markus; Ma, Ke; De Carne, Giovanni; Buticchi, Giampaolo; Blaabjerg, Frede; Liserre, Marco

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2016.2600270

Publication date:
2017

Document Version
Publisher's PDF, also known as Version of record

Thermal Stress Analysis of Medium-Voltage Converters for Smart Transformers

Markus Andresen, *Student Member, IEEE*, Ke Ma, *Member, IEEE*, Giovanni De Carne, *Student Member, IEEE*, Giampaolo Buticchi, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Marco Liserre, *Fellow, IEEE*

***Abstract*—A smart transformer (ST) can take over an important managing role in the future electrical distribution grid system and can provide many advanced grid services compared to the traditional transformer. However, the risk is that the advanced functionality is balanced out by a lower reliability. To address this concern, this work conducts thermal stress analysis for a modular multilevel converter (MMC), which is a promising solution for the medium voltage stage of the ST. The focus is put on the mission profiles of the transformer and the impact on the thermal stress of power semiconductor devices. Normal operation at different power levels and medium voltage grid faults in a feeder fed by a traditional transformer are considered as well as the electrical and the thermal stress of the disconnection and the reconnection procedures. For the validation, the thermal stress of one MMC cell is reproduced on a laboratory setup with high-speed temperature measurement. It is concluded that the investigated conditions, including inrush currents and power variations, do not cause a significant lifetime reduction.**

***Index Terms*—Power converter, power electronics, reliability, smart transformer (ST).**

I. Introduction

A GLOBAL trend goes to increased distributed power generation, which is typically fed into the distribution grid at medium voltage level. This changes the concept of large centralized power plants for which the actual electrical distribution system is designed [1], [2]. On the one side, the variable power generation is causing bidirectional power transfer in parts of the grid, which challenges the controllability and the protection systems, and on the other hand, in many countries the production and the consumption of the power is geographically dispersed. Here, the time varying renewable energy production in combination with the long distances between generation and consumption challenges the grid management. The energy managing capability of the grid with the present transformer is limited and a smart transformer (ST), which is based on power electronic converters with communication and intelligent grid management capability, can provide additional services and improve the controllability to meet the future challenges of the distribution grid [3], [4].

The ST has been proposed for traction applications, where its efficiency outperforms the traditional 16.7 Hz transformer, but still it has not achieved market breakthrough [5]. In the distribution grid instead, the advantage of additional services is motivating the application of the ST. However, even if the power electronics have become a consolidated technology, its reliability is still considered to be lower than the traditional transformer, which typically has a lifetime of 50 years. This makes the reliability an important research topic for designing reliability competitive STs under the consideration of its stress in the grid. In the existing literature, there is an analysis of the efficiency of different modular ST topologies, which is dependent on the number of power semiconductors and power/voltage levels [6], but for the reliability of the ST, there is a lack of knowledge. A study has investigated the ac side stability under dc-line faults [7], but the thermal stress of the used power semiconductors considering the mission profile has not been investigated.

The mission profile of the ST is characterized by partial load operation, possible bidirectional power flow, which puts stress on the antiparallel power semiconductors and the services provided to the grid [8]. In contrast to other applications, the ST enables to partially shape its mission profile by providing services to the grid, which are not mandatory to the current state, but put loading on the devices [2]. The existing research for reliability is mainly limited to the studies of component counts and redundancy, whereas the actual operating status or mission profiles like the control behaviors or the grid conditions are often neglected [9].

For the reliability analysis, a physics-of-failure approach is of importance to apply, and it is possible to use mission profiles of one transformer in the grid to simulate how the semiconductors are stressed in the ST and thereby calculate the expected lifetime [10]. However, the thermal cycling for the power electronics in ST applications has not been investigated for an medium voltage converter under different loading conditions and grid faults.

This work briefly reviews severe grid conditions and components, which can fail in power electronic converters. Among the most fragile components, there are the power semiconduc-

Manuscript received June 7, 2016; accepted August 7, 2016. Date of publication November 14, 2016; date of current version February 11, 2017. This work was supported by the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013)/ERC under Grant 616344—HEART. Recommended for publication by Associate Editor J. H. Enslin.

M. Andresen, G. De Carne, G. Buticchi, and M. Liserre are with the Chair of Power Electronics, Christian-Albrechts University of Kiel, Kiel 24118, Germany (e-mail: ma@tf.uni-kiel.de; gdc@tf.uni-kiel.de; gibu@tf.uni-kiel.de; liserre@ieee.org).

K. Ma is with the School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: kema@sjtu.edu.cn).

F. Blaabjerg is with the Department of Energy Technology, Aalborg University, Aalborg East 9220, Denmark (e-mail: fbl@et.aau.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2600270

tors, whose failure mechanisms are based on thermal cycling. Applying the physics of failure approach, the thermal stress for a medium voltage side modular multilevel converter (MMC) [11] of a three-stage ST solution for the distribution grid system is investigated. The main focus is put on the thermal stress of the power semiconductor devices during normal operation with bidirectional power flow. Furthermore, a grid fault in a feeder connected to the distribution grid seen by a traditional transformer is investigated. The results are validated by emulating the loading of an MMC cell during the grid fault with an H-bridge converter built of an open insulated-gate bipolar transistor (IGBT) module.

First, the studied MMC-based ST architecture is introduced in Section II, failures and possibly faulty components are reviewed in Section III. The investigated grid and the mission profiles for an ST in the distribution system are described in Section IV, whereas the thermal and lifetime models are described and evaluated in Section V. This is continued damage accumulation for these profiles in Section VI and with its lifetime analysis in Section VII. Section VIII emulates the thermal profile of one MMC cell on an laboratory setup and finally, Section IX concludes the work done.

II. ST Under Study

The solid state transformer (SST) is an ac/ac power electronics converter that features galvanic isolation. Motivated by the advantage of reduced space requirement, the SST has been proposed for traction applications [12], where it outperforms the $16.7-\mathrm{Hz}$ transformer [5]. However, with the advancement of technology, more intelligence can be embedded into the converter, as well as communication capability, which is not beneficial in the traction application. Instead, it is potentially advantageous for the connection of the medium voltage (MV) grid with the low voltage (LV) grid [13]–[16]. The SST can provide ancillary services for the grid and potentially controls loads and generation. As an additional feature, it can provide direct dc-link access for the connectivity of dc grids [17]. The embedded intelligence in the power converter leads to a more suitable name of the SST, the ST.

A. Smart Transformer and Its Functionality

Independently from the various ST topologies proposed in literature [18], [19], the functionality is similar. The ST needs to supply the LV feeder while absorbing the necessary active power from the MV grid. Simultaneously, the voltage and the frequency are controlled with constant magnitude and frequency. A control diagram for the ST is shown in Fig. 1.

Since the only constraint is on the active power, arbitrary frequency and amplitude can be chosen for the LV grid. A frequency control allows interacting with the distributed generation, whereas an amplitude variation can partially control the power request.

For the voltage control in the grid, it is mandatory to identify the behavior of the load in response to a voltage variation [20]. As an example, a grid with mainly constant impedance behavior will reduce the power with a voltage reduction, whereas a constant power load behavior will increase the current in that case. Consequently, in order to apply the right control action, the identification of the LV grid is needed.

Unidirectional power transfer from the MV to the LV grid was a good assumption when the distribution grid was designed. However, the reverse power flow can be a problem due to the voltage increase in the MV grid caused by the voltage drop over the transformer and MV lines. In order to avoid this situation, the isolation stage of the ST enables to control the reverse power flow from the LV grid. When the amount of renewable energy in the MV grid is high (e.g., from wind farms or big PV plants), the dc/dc stage of the ST can prevent the power reversal, allowing the dc-link to increase [21]. The dc/ac stage then increases the grid frequency, interacting with the droop controllers of the distributed generation system, forcing them to reduce the output power. The ST sets a new grid frequency (still within the grid code limits), and the active power absorbed from the MV grid is controlled to zero.

The presence of dc-links, both at MV and LV levels, is the key to enable the dc grids: renewables, battery energy storage, and dc loads can be connected to dc microgrids [22].

The reactive power represents a degree of freedom for control: The ST can operate with a unity power factor or can provide ancillary services to the grid by means of reactive power injection. Current and voltage control by means of reactive power injection and harmonic compensation of neighbor feeders [23] are services offered by the ST in the MV grid. By providing the reactive current locally and controlling the voltage amplitude, the total transfer capability of the MV lines increases.

B. MV Converter Stage

The ST can be built with a different number of conversion stages and by different topologies. The single stage ST may be realized with a matrix converter, but the absence of the dc-link would limit the available services. Since ancillary services and dc-connectivity are expected to be the selling argument, this architecture is not viable. A two-stages ST provides dc connectivity either in the low-voltage or the medium-voltage side. However, the highest capability for services is given in the three-stage structure, namely a rectifier, an isolated dc/dc converter, and an inverter as shown in Fig. 1. In this structure, it is possible to interface two different ac power grids with different voltage levels and frequencies. As a result, the three-stage structure of the ST is considered and the medium voltage converter is the object of this paper's investigation.

The MMC topology is a promising solution because of its modularity and industry proofed technology. In this study, an MMC based on half-bridge cells is chosen. As design choices, 15 cells per arm and 1 MW of power are considered (see Fig. 2); Table I lists the parameters of the system. The rated current amplitude is 74.2 A and a voltage stress of 1200 V is selected for the devices. The half-bridge IGBT modules SKM100GB176D (100A/1700V) are selected with a heatsink of P3/180 from Semikron for each cell. It is worth to mention that the optimal design is difficult to be defined because the number of components has strong impact on the device loading and needs to be designed carefully [24]. However, the methods for thermal stress and reliability analysis for the chosen modular system can easily

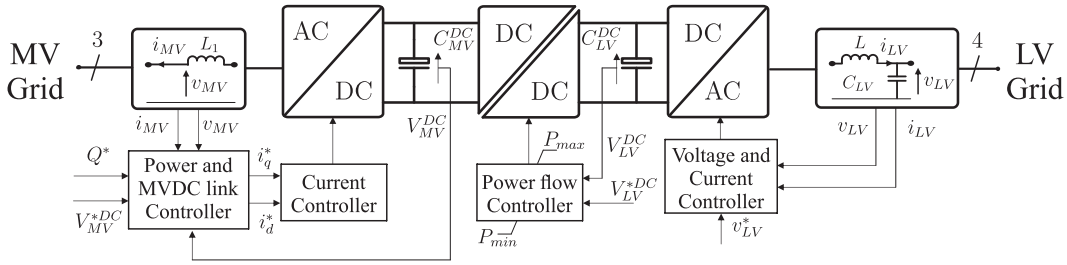

Fig. 1. ST basic control scheme.

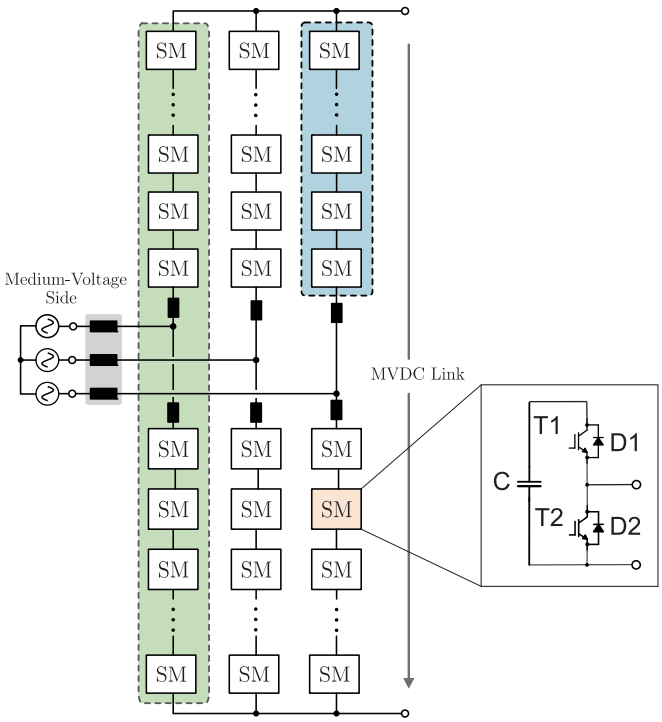

Fig. 2. Modular multilevel converter (MMC) topology for the study case.

TABLE I
PARAMETERS OF THE STUDIED MMC CONVERTER USED IN THIS ST

Rated power	1 MVA
Power factor	1.0
Rated MVDC voltage	19 kV
Rated AC voltage	11 kV rms
Rated load current $I_{\text{load, HV}}$	75 A
Cell number of each arm	15
Fundamental frequency	50 Hz
Switching frequency f_s	2 kHz
Filter inductance L_f	57.8 mH (0.15 p.u.)

be transferred to other designs. It is worth mentioning that the MVDC-link is accessible and there is the possibility to connect to dc grids. The circuit seen in Fig. 2 is modeled based on the Simulink in MATLAB, and a large signal modeling method is applied to speed up the simulation, while preserving the electrical and control behaviors, which are interesting for the thermal analysis.

III. FAILURES IN STS

Based on the physics of failure, each failure of a component needs to be traced until its root cause. Characteristic for the operation of the ST in the distribution grid are the behaviors of the connected MV grids and LV grids. For this reason, the characteristic and the possible conditions, which are stressing components of the ST need to be investigated.

A. Possible MV Events Causing Failures in STs

The stress for the MV grid has increased in the last years due to the penetration of renewables (photovoltaic, wind, etc.,) leading to an increment of disturbances like overvoltages, voltage variations due to faults or fast power variations (e.g., generator disconnection), harmonics, higher short-circuit currents, and flickers.

The voltage response of the grid to a fault in MV grids is dependent on several influencing factors, such as the nature of the fault, the grid composition, and the location of the fault. Overvoltage or undervoltage conditions can be caused by the fault in each phase, depending on the grounding adopted in the grid [25]. A well-earthed neutral system leads to high short-circuit currents, which is limiting the overvoltages, but it requires the installation of big short-circuit breakers. This is usually adopted in high-voltage (HV) transmission grids. In ungrounded systems, a temporary overvoltage (till $2.5 - 3$ pu) can occur during a single-phase fault contingency [26]. If the system is grounded by means of a Petersen coil or a suppression coil (e.g., in Germany), the overvoltage can be reduced to 1.8 p.u. For the power semiconductors, overvoltages need to be limited in magnitude, because exceeding the rated collector emitter voltage causes immediate destruction of the device. Undervoltages can also occur during a fault. As observed in [27], the junction temperature of power semiconductor components increases significantly with the magnitude of the voltage dip. The temperature also depends on the type of fault (single-, two- or three-phase fault). Providing services like the reactive power injection for voltage support can affect the lifetime of the component. As shown in [28], the injection of reactive power increases the thermal cycling of each component, increasing the losses and impacting on the lifetime of the devices.

B. ST Components and Their Failure Mechanisms

The power converter is built by several components, which can possibly fail (see Table II). In order to identify the most frequently failing components, a survey was made in [29]. This survey identified the power semiconductors to be the component with the highest probability for a failure. Among the three most fragile components were listed capacitors and gate drivers. Others are connectors, printed circuit board (PCBs), inductors,

TABLE II
ST COMPONENTS AND MV OCCURRENCES, WHICH COULD AFFECT THEM

MV-side ST components	MV occurrences
Power semiconductors	Power variations
DC-link Capacitors	Harmonics
Fuses	Power variations
Inductors (Filter)	Low failure probability
Driver circuits	No interaction with the grid

resistors, and fuses. In order to apply the physics of failure approach, the real operating conditions are used to identify the mission profile of the components. The most relevant failure mechanisms of the power semiconductors are related to thermal cycling [30].

C. Analysis of the Most Thermally Stressed Components of the ST

As described in the last section, power semiconductors are the most frequently failing components in power converters. For this reason, the physics of failure approach requires to perform thermal stress analysis based on the mission profile, which is translated into thermal cycles and the damage, which is translated into the lifetime of the system. Due to the different coefficients of thermal expansion within the commonly used direct bonded copper structure of the power electronic modules, a variation of the temperature causes mechanical stress. The common failures in power electronic modules are found at the bond wires and the interconnections within the modules, namely chip solder, base plate solder, and bond wire liftoff. The mechanisms, which cause the wear out are based on the temperature swing, which needs to be separated from the temperature profile. A common way to do is to apply thermal cycle counting, such as rainflow counting. From the counted cycles, there are models to derive the thermal stress and the accumulated damage. One of the models taking into account this failure mechanism is the LESIT lifetime model based on the accelerated tests of IGBT modules leading to solder fatigue [31]. The data are only available for limited thermal swings between $\Delta T = 30$ K and $\Delta T = 80$ K, but in this work the range is linearly extrapolated in the logarithmic scale to smaller magnitudes. Furthermore, the technology has proceeded and there are new IGBT technologies, which are having higher thermal cycling capability. Nevertheless, the failure mechanisms and the dependence on the temperature swing remains [30]. Based on the LESIT models, the accumulated damage is derived from the rainflow counted cycles. In this work, thermal swings with amplitude smaller than 1 K are neglected.

Capacitors, as the second most fragile components, undergo thermal stress affected by harmonics [32]. Since this is not connected to the failure mechanism of the power semiconductors and requires another analysis, this work focuses on power semiconductors.

IV. MISSION PROFILES OF THE ST

The ST undergoes power flow variations, which are caused by the variation of the load and the power generation in the connected grid feeders. These power variations are representing the normal operating conditions of the ST, which need to be carefully considered. Another stressing conditions is caused by variations in the grid voltage and can even lead to a disconnection of the ST to prevent its damage. These grid voltage variations can occur in the medium voltage grid side or low voltage grid side of the ST. In the following, the power grid configuration under investigation is described first and afterward the thermal impacts to the power semiconductors caused by normal operation and the grid faults conditions are examined.

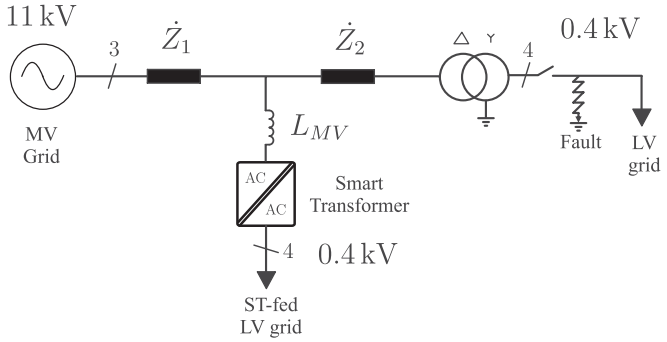

Fig. 3. Investigated MV grid with an ST feeding a LV grid and a feeder connected by a traditional transformers.

A. Description of the Investigated Grid

For simulating the thermal stress of the MMC in the distribution grid, an ST is considered to be installed in the medium voltage grid. It is interfacing a low-voltage ac grid feeder as shown in Fig. 3. The power of the investigated feeder is 1 MVA, whereas the ST is sized as described in Table I. The ST is located in a distance of 2 km to the feeder of the MV grid and another low-voltage grid is connected to the same MV feeder by a conventional transformer in a distance of 1 km to the ST.

The low-voltage grid, which is fed by the ST is composed of connected photovoltaic power generation (PV), wind power generation, and loads. It is assumed that the medium-voltage side converter does not generate reactive power for the medium-voltage grid and operates with $\cos(\varphi) = 1$, whereas the low-voltage side converter of the ST is transferring reactive power into the low-voltage grid. However, the reactive power in the low-voltage grid is not affecting the MMC converter of the ST at the medium voltage side.

B. Power Flow Variations

The ST has to operate in several different conditions, whereby it is expected to operate in partial load operation for most of the time and to be objected to daily periodic cycles as shown in Fig. 4(a). Due to the power generation in the LV grid, the power flow can be bidirectional, which is changing the stress distribution between the power semiconductors. The first scenario shown in Fig. 4(b) is characterized by high power consumption of the loads in the LV grid and low power production by the renewable power plants, which will result in high power flow from the medium-voltage grid into the low-voltage grid. The second scenario in Fig. 4(c) shows the medium power consumption by

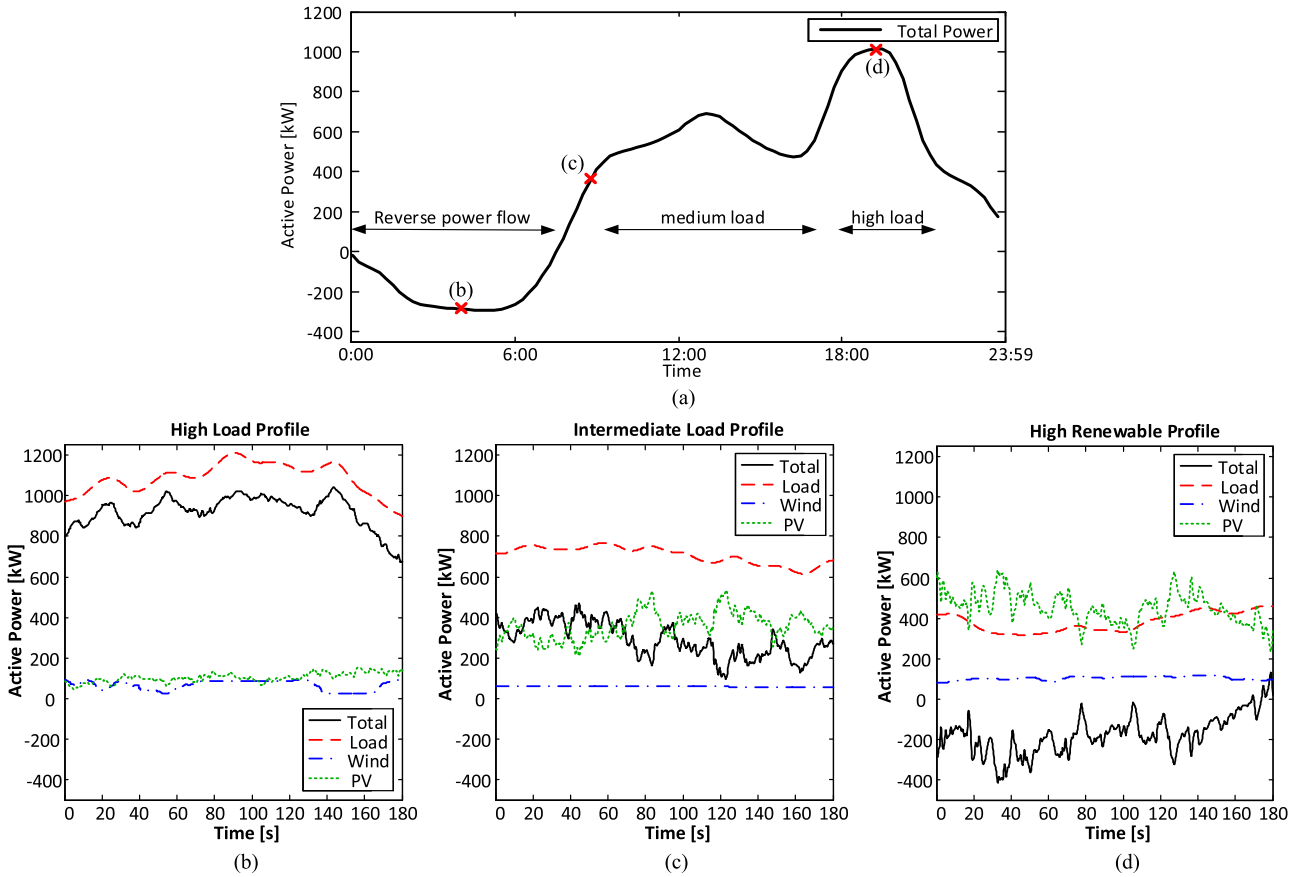

Fig. 4. Load profile for the study with active power in a grid: (a) High load and low generation. (b) Medium load and medium generation. (c) Low load and high generation.

the loads on LV side and medium power generation in the LV grid. This is expected to be the most of the loading condition of the ST and it results in a medium power transfer from MV grid into the LV grid. The third scenario is characterized by high power production of the renewable sources on the LV side and low consumption by the connected loads of the LV grid. It results in bidirectional power flow and higher fluctuations of the power.

C. Grid Faults

Special attention is put on the loading of the power semiconductors in the MV stage of the ST during grid faults in low-voltage feeders fed by the traditional transformer. A fault in the low-voltage grid can cause voltage sags in the MV grid, which influence all connected feeders. In particular, the ST is reacting to voltage variations like a constant power load, which increases the transferred current and thus increases the stress for the power semiconductors. In case of a HV sag, the feeder needs to be disconnected. Additionally, the reconnection of the LV grid feeder after a tripped breaker causes inrush currents for the transformers. These inrush currents will stress the MV grid by injecting a zero sequence current with a magnitude, which can be several times higher than the nominal current designed for [33]. Due to the limited overloading capability of power semiconductors, this case is studied for the three-phase short circuit on the LV grid side grid fed by the traditional transformer. A three-phase short circuit in the low-voltage grid does not have the highest probability, but the biggest impact on the grid in terms of voltage sags. For this reason, it is taken as the worst study case to demonstrate the influence of faults in feeders of the ST connected to the same grid. The position of the fault occurrence is shown in Fig. 3.

The disconnection and reconnection procedure of this transformer after a fault is described in Fig. 5. In this study, the fault occurs after 1s of the simulation and 0.3s later the breaker is activated. After additional 0.3 s, the breaker is closed to test if the fault is cleared. This closing induces an inrush current in the transformer of the reconnected grid, because it is not magnetized. However, due to the uncleared fault, the breaker reopens after 0.3 s and reopens again after 3 s to test if the fault is cleared. In the meantime the fault is cleared. Thus the breaker is closed, causing another inrush current in the transformer and then the grid is back to normal again.

The fault in the connected feeder influences the current and voltage profiles of the ST. During faults, the impedance of the transformer and the strength stiffness of the MV grid determine the short-circuit current. This short-circuit current is causing a voltage drop on the transformer and causes a voltage dip in the medium voltage before the breaker opens. Since the ST is

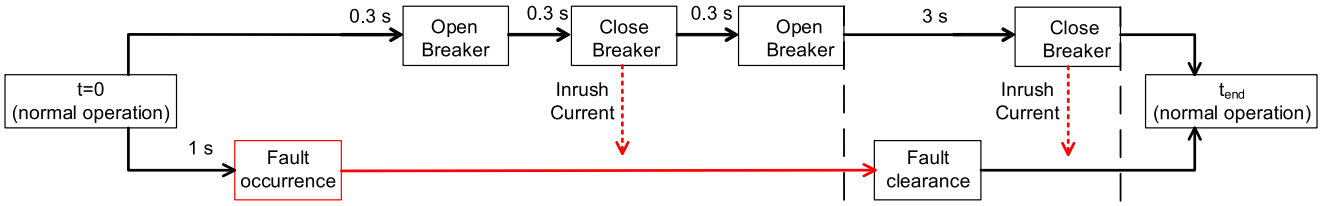

Fig. 5. Grid reconnection procedure after a fault using the breaker in Fig. 3.

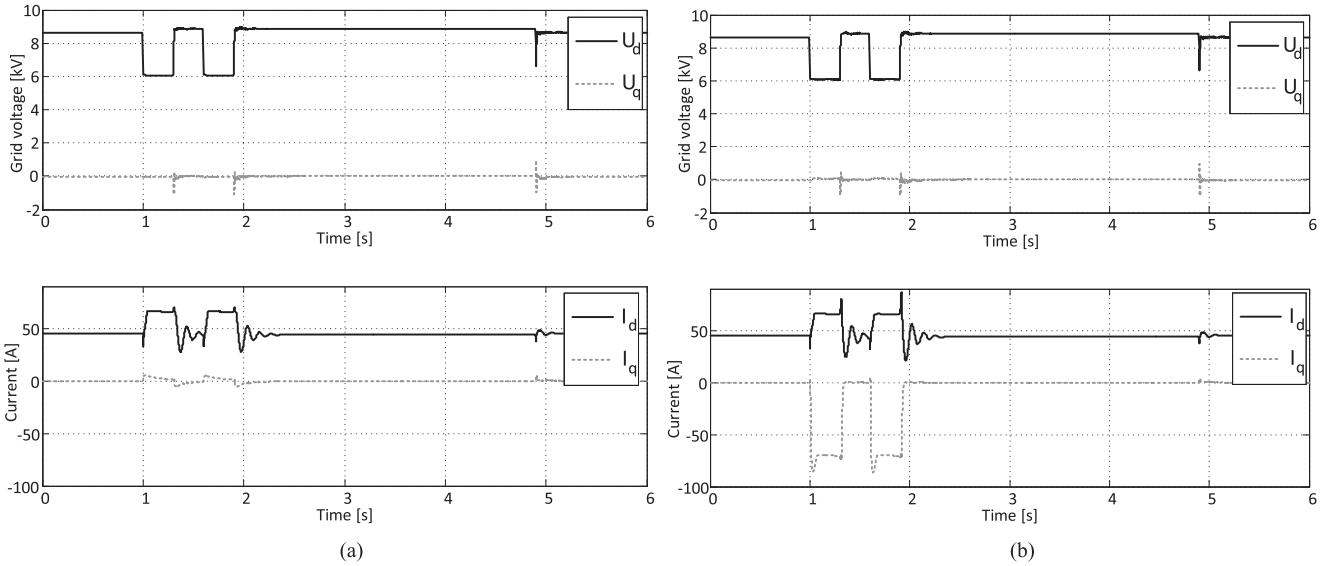

Fig. 6. Current and voltage profile of the ST during a three-phase MV grid fault and reconnection procedure: (a) for normal ST operation, (b) for reactive current injection.

behaving like a constant power load, which is different with respect to the traditional transformer, the current on the MMC is increasing. The characteristic behavior of the grid voltage and current during the three-phase short circuit is presented in Fig. 6. In Fig. 6(a), the medium-voltage-side ST voltage and current during the investigated grid fault are shown. In this case, the ST is behaving like a constant power load, but does not actively react on the fault. Instead, it is still feeding the low-voltage grid feeder and the current is increased because of the drop in voltage. In Fig. 6(b), the ST is injecting reactive current to support the grid voltage, which results in a significantly higher output current of the ST. This higher output current is expected to cause higher losses and thus higher thermal stress for the power semiconductors.

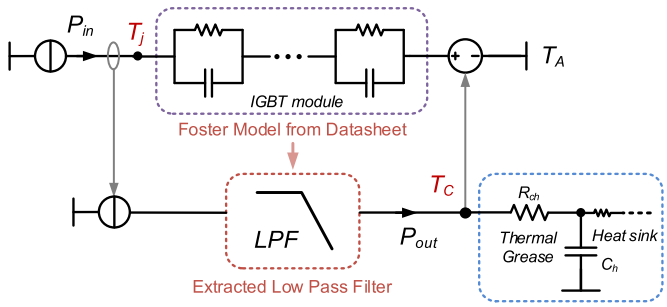

Fig. 7. Applied thermal model for power device modeling.

V. Thermal Stress Evaluation

A. Thermal Modeling

Based on the operating conditions, design and control methods for each stage of the ST, the loading conditions of the devices can be estimated with proper loss and thermal models. The loss model used has the same idea as in [34], which is a commonly accepted method for the loss evaluation of power semiconductor devices. Because the thermal behaviors are modeled based on the relatively long-term mission profiles as shown in Fig. 4, the accurate temperature estimation outside the power device, which has much slower thermal dynamics than the internal junction temperature, are important. Unfortunately, as discussed in [35], both the widely used Cauer and Foster thermal models for power semiconductor devices have their limits to acquire the appropriate case and heat sink temperature outside the power device. As a result, a new thermal model proposed in [35] is applied. As shown in Fig. 7, the new thermal model contains two paths: the first thermal path is used for the junction temperature estimation. In this path, the datasheet-based

multilayer Foster thermal network inside power devices are used, and only a temperature, whose value is determined by the case temperature T_c from the other thermal path, is connected to the Foster network. As a result, the Foster network is correctly used and an abrupt change of case/junction temperature can be avoided. The second thermal path is used for the case and heat sink temperature estimation. In this path, the thermal network inside the IGBT module is just used for the loss filtering rather than for the junction temperature estimation, and the complete thermal network outside the IGBT module (i.e., thermal grease and heat sink) is included. It is noted that the multilayer Foster network inside the IGBT module is mathematically transformed to a low-pass filter for the power loss. As a general case, it is assumed that the ambient temperature of the converters for the study $T_a = 40$ °C. In order to achieve a relatively conservative design and to ensure certain reliability for each stage of the ST, the heat sink is designed to maintain a temperature below 60 °C, and the power semiconductors are selected to achieve a junction temperature around 80 °C. Since the power profile exceeds the rated power for short time periods, the maximum temperature is also expected to exceed 80 °C.

B. Thermal Stress for the Converter During Normal Operation

For the thermal stress analysis during normal operation, the three mission profiles shown in Fig. 4 are simulated. In Fig. 8, the junction temperature of all power semiconductors in one half-bridge are shown. These temperature profiles are also valid for the power semiconductors in the other half-bridge cells in the MMC converter. The first profile leads to junction temperatures between 60 and 85 °C. The IGBT T1 and the diode D1 in the half-bridge cell are the most stressed devices in this condition and the maximum junction temperature is in accordance with the design. T1 shows a thermal swing of $\Delta T \approx 4$ K in the fundamental period, while T2 is stressed less with $\Delta T \approx 3$ K. The diodes obtain approximately the same temperature swing of $\Delta T < 1$ K. In the second profile [see Fig. 4(c)], the average temperature is remarkably reduced for all power semiconductors and the temperature swing is much lower than in the first profile. Especially the stress for the diodes D1, D2, and transistor T1 are significantly reduced. The third profile [see Fig. 4(d)] with reduced load and bidirectional power flow shows further reduction of the mean temperatures of T1, D1, and D2. The IGBT T2 is now more loaded than T1 and the diodes undergo higher thermal cycles than in the previous case. This is mainly caused by the high power generation of the renewable sources, which causes high-power fluctuations.

C. Effect of the Fault on the Lifetime of the Power Modules

The voltage and current profiles shown in Fig. 6 are now being simulated to evaluate the thermal stress for the power semiconductors. This results in the junction temperature profiles shown in Fig. 9 for the case without reactive power injection and for the case with reactive power injection. In both cases, the fault causes increased thermal cycles. These increased thermal cycles occur during the fault and during the first closing of the breaker when the fault is not cleared. The thermal swing is relatively low, because the time until the breaker opens is short, even in comparison to the time constants of the thermal impedance of power device and heat sink. Of course, there are situations in which the voltage in the grid is even lower than in the simulated case, but this is very rare in grids with high standards. Remarkably, the effect of the inrush currents on the ST is not even visible in the junction temperature profile of the ST. As a result, the inrush currents in parallel feeders do not affect the stress for the ST.

VI. Thermal stress evaluation of the ST

The thermal profiles from Section IV are used to compute the consumed lifetime of the power semiconductors, which is also defining the lifetime of the power converter. The most stressed power semiconductor, which was identified in Section V, is now considered and rainflow counting is applied for its junction temperature profile.

A. Thermal Stress Evaluation During Normal Operation of the ST

In Fig. 10, rainflow counting is applied for the IGBT T1 in the MMC half-bridge cell, which is the most stressed power semiconductor in this topology. Most thermal cycles in all load conditions are generated by the fundamental frequency, which can be identified by the density of cycles with similar amplitudes. The other thermal cycles are generated by the load profile and some are visible as steps in the accumulated damage [see Fig. 10(b), (c)]. The accumulated damage is added, when the thermal cycle is completed. The total consumed lifetime is highest for the high-load profile, whereas the others obtain almost similar consumed lifetime. Nevertheless, their consumed lifetime is much lower than the consumed lifetime of the high-load profile.

B. Thermal Stress Evaluation of the Fault

To identify the magnitude of the thermal cycles during the fault, rainflow counting is applied to the temperature profile of Fig. 9. The magnitude of the largest thermal cycles without reactive current injection is approximately 6.5 K, whereby in the case with reactive current injection, the thermal swing is increased to 8 K. This has limited influence on the lifetime of the ST, as can be seen in the damage for both cases. Even if the damage for the injection of reactive current is two times higher than in the first case, the overall damage is still low. Remarkably, the inrush currents of the reconnection procedure can neither be identified in the thermal profile of the power semiconductors nor in the rainflow counted cycles. This leads to the conclusion the inrush current do not influence the lifetime of the ST.

In the case of a blackout of the medium voltage grid, the reconnection of the low voltage feeder is usually coordinated in

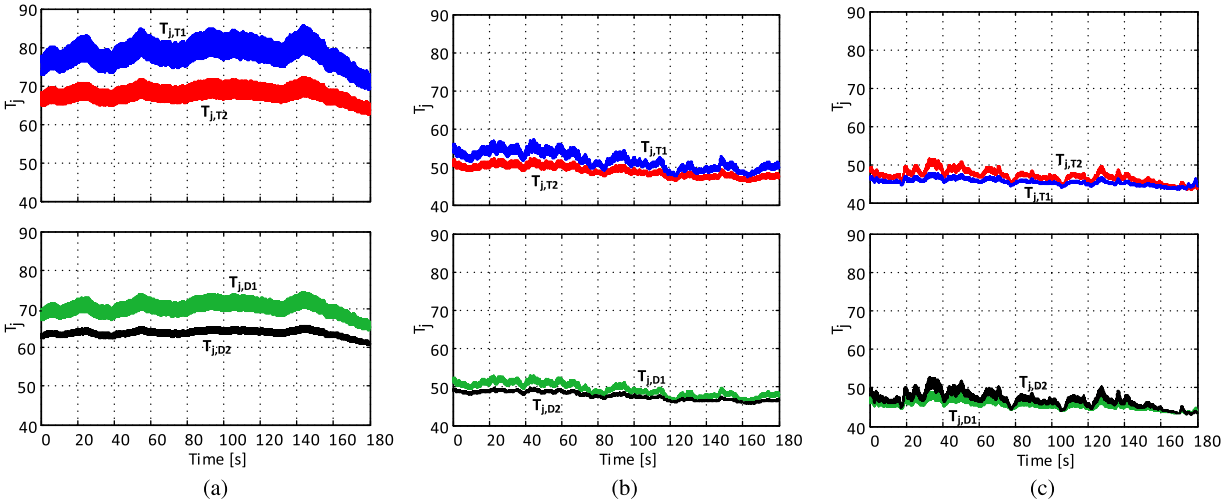

Fig. 8. Thermal stress for the MMC during the different loading conditions: (a) High load and low generation. (b) Medium load and medium generation. (c) Low load and high generation.

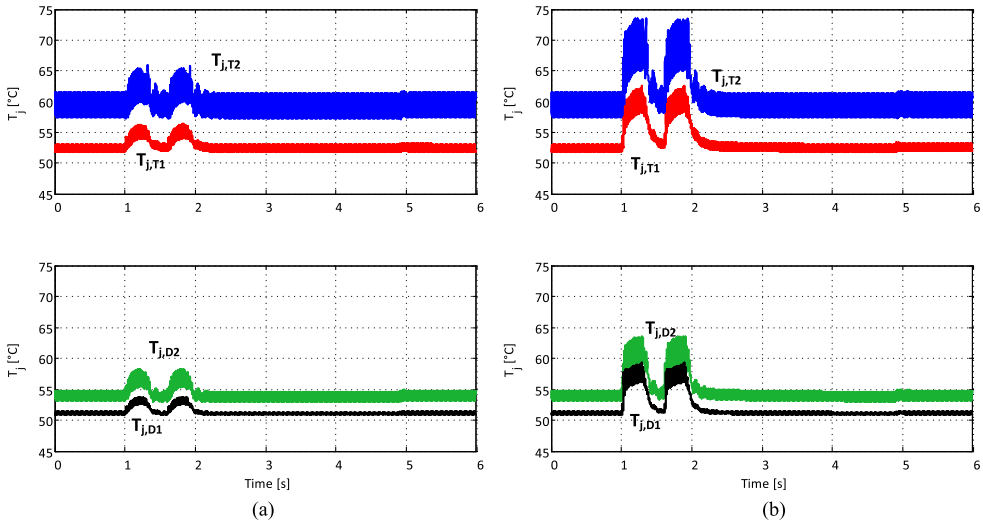

Fig. 9. Junction temperatures of one cell during fault and reconnection procedure: (a) for normal ST operation, (b) for reactive current injection.

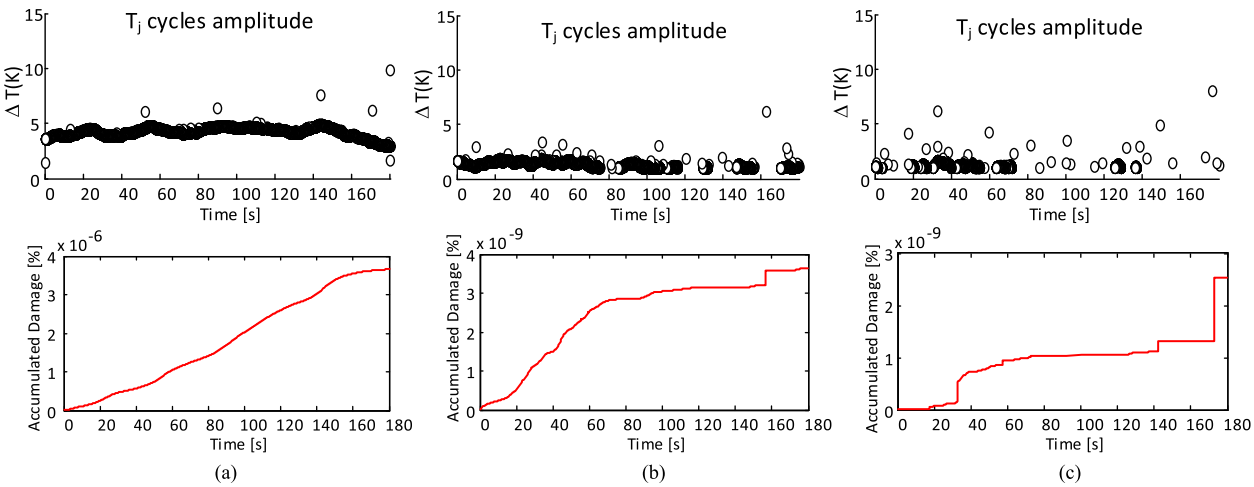

Fig. 10. Rainflow cycle counting and accumulated damage of the bond wire for the junction temperature of T1 in the MMC during the different loading conditions: (a) High load and low generation. (b) Medium load and medium generation. (c) Low load and high generation.

TABLE III
PARAMETERS FOR THE TRANSLATION FROM THERMAL STRESS TO LIFETIME

Occurrence	Assumed occurrence	Effect on lifetime %
Short term power variations:	minutes	
under high load [as in Fig 4(b)]	10% of time per day	89.8
under medium load [as in Fig 4(c)]	65% of time per day	0.6
with reverse power flow [as in Fig 4(d)]	25% of time per day	0.2
Working day consumer behavior as shown in Fig. 4(a)	5 cycles per week ($\Delta T = 45$ K)	0.9
Weekend consumer behavior	2 cycles per week ($\Delta T = 30$ K)	0.1
Weather and wind variations affecting the generation	12 cycles per week ($\Delta T = 55$ K)	5.8
Weather and wind variations affecting the generation	2 cycles per week ($\Delta T = 65$ K)	2.2
Ambient temperature variations	2 cycles per month ($\Delta T = 70$ K)	0.8
	2 cycles per year ($\Delta T = 90$ K)	0.2
Grid faults		
without disconnection [as in Fig. 6(b)]	1 per week with damage from Fig. 11(b)	0.1
with disconnection of the grid	1 per month with $\Delta T = 50$ K	0.4

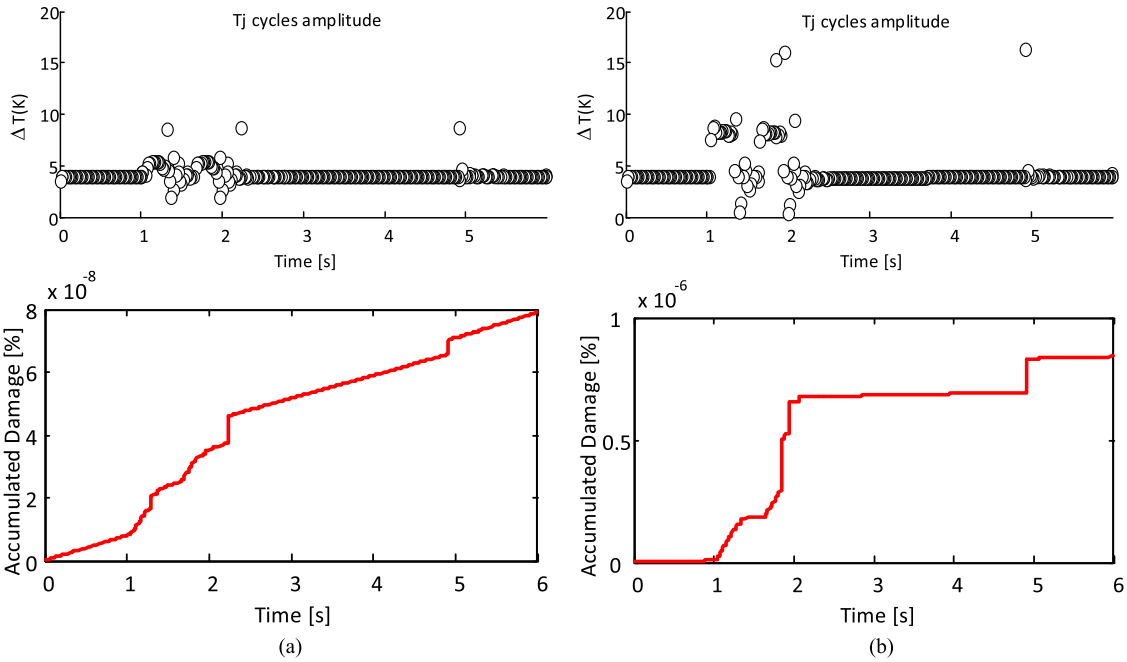

Fig. 11. Rainflow cycle counted for junction temperature and accumulated damage of the bondwire for one IGBT in the MMC during the grid fault: (a) without reactive current injection, (b) with reactive current injection.

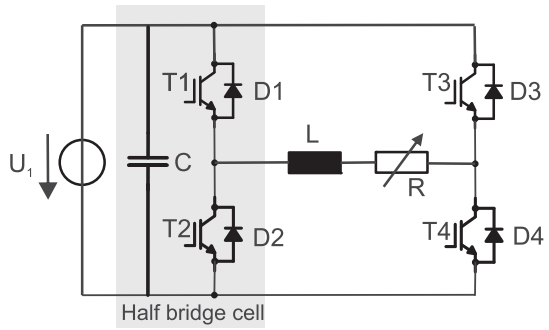

Fig. 12. H-bridge converter for the emulation of the power semiconductor stress in one MMC cell.

time. Thus it is prevented, that the effects of the reconnection, such as inrush currents, are accumulating and result in high damage.

VII. LIFETIME EVALUATION OF THE ST

Based on the thermal simulations, the thermal stress needs to be translated into the lifetime of the MMC in the distribution grid. It needs to be pointed out that this is highly dependent on the load profile and thus on the connected loads and generators. In this study, the profile of Section IV-B with high power, medium power, and reverse power flow is assumed to repeat daily. Since the thermal simulations are made for short time periods of 3 min, it needs to be extrapolated to cover the whole time in operation. Furthermore, periodic or statistic occurrences needs to be estimated to identify factors affecting the lifetime of the system. Examples for stressing factors are thermal cycles caused by daily power variations (e.g., caused by consumer behavior, factories, or generation), sun/-wind variation affecting the renewables, ambient temperature variations affected by weather variations and faults. In Table III, the assumed parameters are shown. For only 10% of the time full load operation

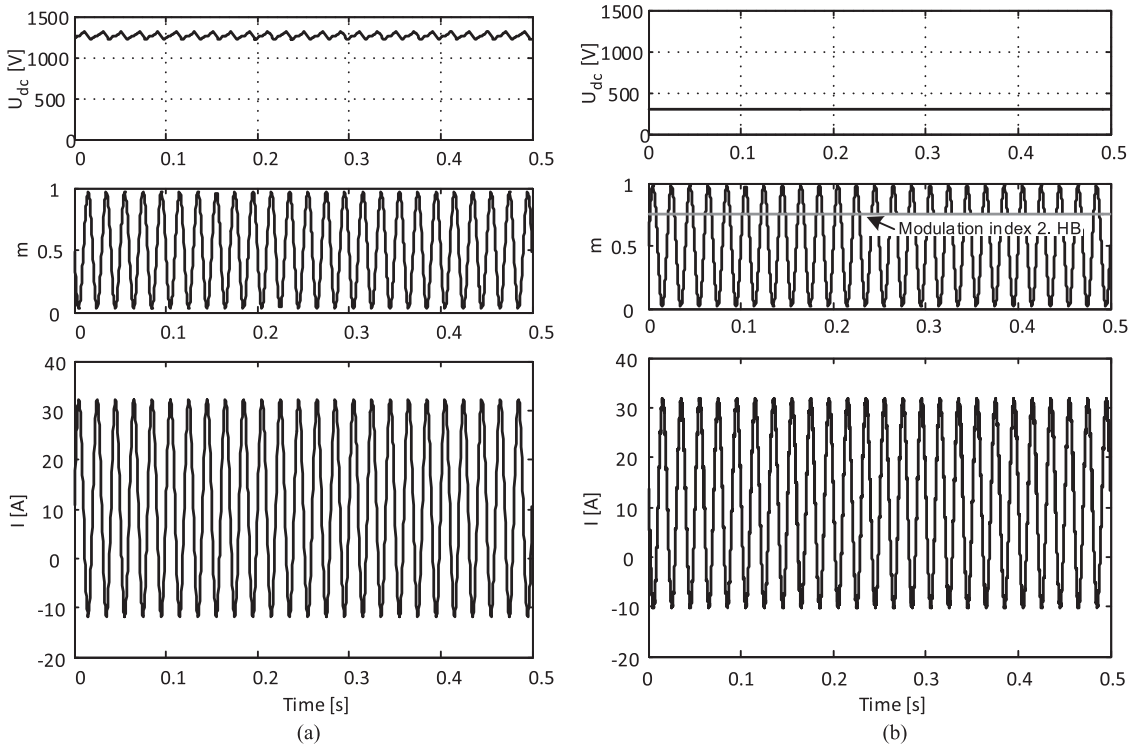

Fig. 13. Comparison of electrical characteristics between: (a) MMC cell voltage and current and (b) H-bridge voltage and current for reduced dc-link voltage and modified modulation.

TABLE IV
PARAMETERS OF THE EXPERIMENTAL SETUP FOR THE MMC CELL EMULATION

Cell voltage	300 V
Switching frequency	20 kHz
Rated rms cell current	25 A
load inductance	2 mH
load resistance	7 Ω
load resistance during voltage sag	4 Ω

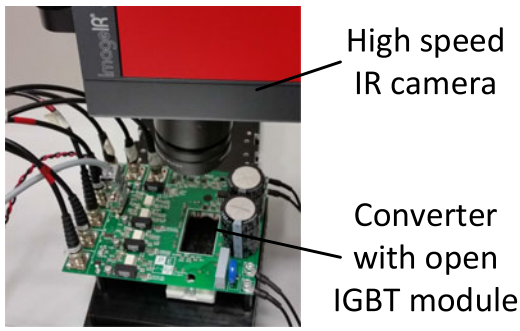

Fig. 14. Laboratory setup with IR camera and open IGBT module.

is assumed, while medium power is assumed for 65% of the time and reverse power flow for 25% of the time. For every working day per year, a thermal cycle of 45 K is assumed and for the weekend a thermal cycle with the magnitude of 30 K. Additional cycles are assumed to be affected by variation of the renewable generations, ambient temperature variations, and grid faults. In case of grid faults, it is distinguished between the simulated case with reactive current injection and the case of feeder disconnection, which results in a total cooling down of the power semiconductors.

It is shown that the highest influence on the lifetime is caused by the high loading profile with almost 90% of the lifetime consumption. The second highest influencing factor with 8% is caused by the fluctuation of the generated power of the renewable generation. All other effects have low influence on the lifetime of the ST. The considered operation conditions lead to a high lifetime expectation and no particular limiting factor is found.

VIII. EXPERIMENTAL VALIDATION OF THE THERMAL STRESS

To validate the thermal stress of an MMC cell, one MMC half-bridge cell (as shown in Fig. 12) is used in an H-bridge setup for emulating the current profile of power semiconductor in an MMC cell. For the evaluation, an open IGBT power module (Danfoss DP25H1200T101667-101667) is used in the setup, which requires to operate the cells with reduced dc-link voltage due to the absence of the gel in the module. The junction temperature is measured with a high-speed infrared camera and the grid voltage drop is emulated with an electronic load by reducing its resistance. The half-bridge, which emulates the MMC cell is driven with the same modulation signal as the MMC cell, while the second half-bridge in the H-bridge is operating with a constant duty cycle of 0.75. This results in the same turn on times and the conduction times as for the power semiconductors

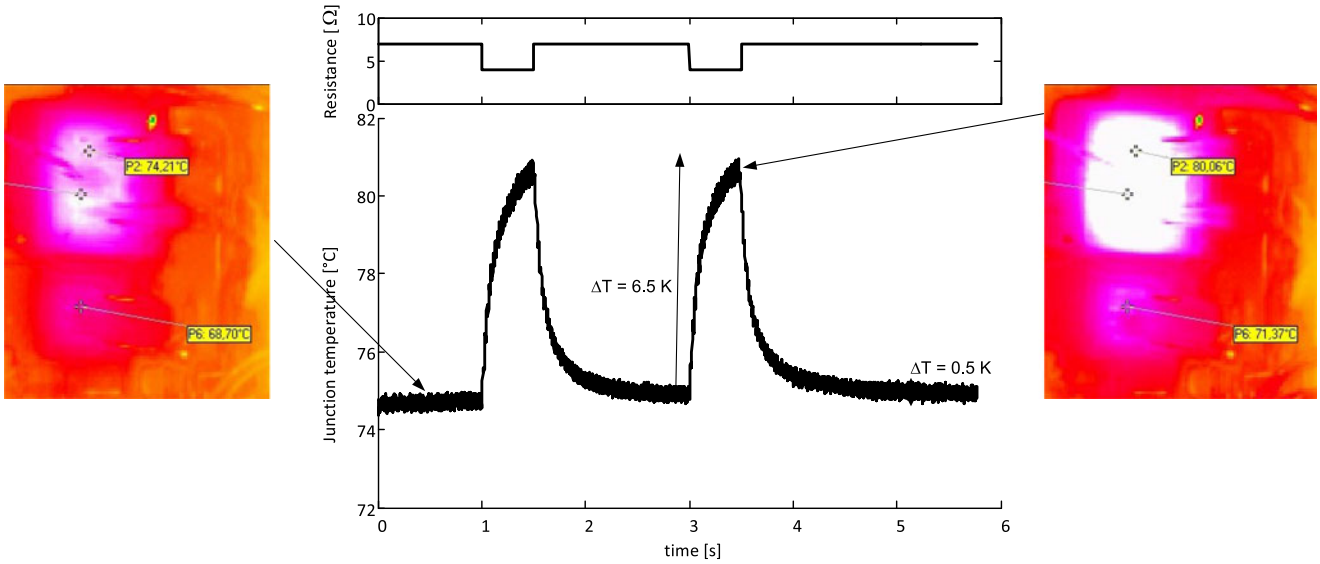

Fig. 15. Laboratory measurement: Junction temperature measurement of one IGBT during the emulation of the investigated grid fault.

in the MMC cell. The parameters of the H-bridge are shown in Table IV.

To demonstrate that the electrical characteristics of one MMC cell and the H-bridge are similar, Fig. 13(a) shows the electrical characteristics of the MMC cell, while the corresponding measures of the H-bridge cell are presented in Fig. 13(b). The dc-link of the MMC cell shows an oscillation, which is not reconstructed in the full-bridge, but this oscillation is relatively lower, which makes it negligible for the loading of the device. With the same modulation signal, the voltage and current of both cells show approximately similar ac and dc components.

The H-bridge setup shown in Fig. 14 is used to emulate the behavior of one MMC cell during operation and the described voltage sag. The converter is driven in steady state to obtain a stationary temperature distribution on the surface of the power electronic module. To emulate the voltage sag, the resistance is changed stepwise from $R = 7\ \Omega$ to $R = 4\ \Omega$ for 0.5 s. The results of the recorded thermal profile are shown in Fig. 15. The thermal cycles in the fundamental period have a magnitude of $\Delta T = 0.5$ K and during the voltage sag the temperature is cycling with $\Delta T = 6.5$ K. It can clearly be seen that the power semiconductor is heated up during the power cycle. Both thermal swings are lower than in the simulations, but show the same characteristic behavior. A possible explanation is the use of passive heatsinks without fans in the setup, which results in a higher thermal resistance compared to actively cooled devices in the simulation.

IX. Conclusion

The thermal stress for an MMC converter connected to the medium voltage distribution grid as the first stage of an ST has been investigated. Three different loading conditions have been simulated and a grid fault causing inrush currents and a drop in the medium voltage grid are analyzed in combination with the constant power behavior of the ST. The thermal profiles of the different conditions have been presented and the accumulated damage has been derived and translated into the lifetime of the system. Even if the thermal stress caused by grid faults is higher than in normal operation, no significant decrease of lifetime has been found. Neither the inrush currents nor the normal operation causes severe thermal stress. In the considered grid conditions, the high load operation was causing approximately 90% of the lifetime consumption. The thermal stress in one MMC cell was reproduced for the investigated grid fault on a laboratory setup in an H-bridge converter with the resultant thermal cycles of the power semiconductors.

References

[1] B. K. Bose, "Global energy scenario and impact of power electronics in 21st century," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2638–2651, Jul. 2013.

[2] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z.-X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Ind. Electron. Mag.*, vol. 10, no. 2, pp. 46–58, Summer 2016.

[3] G. De Carne, M. Liserre, K. Christakou, and M. Paolone, "Integrated voltage control and line congestion management in active distribution networks by means of smart transformers," in *Proc. 2014 IEEE 23rd Int. Symp. Ind. Electron.,* 2014, pp. 2613–2619.

[4] J. Posada Contreras and J. M. Ramirez, "Multi-fed power electronic transformer for use in modern distribution systems," *IEEE Trans. Smart Grid*, vol. 5, no. 3, pp. 1532–1541, May 2014.

[5] J. W. Kolar and G. Ortiz, "Solid-state-transformers: Key components of future traction and smart grid systems," in *Proc. Int. Power Electron. Conf.*, Hiroshima, Japan, 2014.

[6] A. L. Kirsten, T. H. de Oliveira, J. G. Roncalio, C. Rech, and M. Dalla Costa, "Performance analysis of modular converter for solid state transformers," in *Proc. 2013 Brazilian Power Electron. Conf.*, 2013, pp. 1060–1066.

[7] G. Tang, Z. Xu, and Y. Zhou, "Impacts of three MMC-HVDC configurations on ac system stability under dc line faults," *IEEE Trans. Power Syst.*, vol. 29, no. 6, pp. 3030–3040, Nov. 2014.

[8] B.-M. Han, N.-S. Choi, and J.-Y. Lee, "New bidirectional intelligent semiconductor transformer for smart grid application," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4058–4066, Aug. 2014.

[9] H. Wang *et al.*, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 97–114, Mar. 2014.

[10] N.-C. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, and P. de Place Rimmen, "Reliability oriented design tool for the new generation of grid connected PV-inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2635–2644, May 2015.
[11] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. 2003 IEEE Bologna Power Tech Conf.*, 2003, vol. 3, pp. 1–6.
[12] D. S. Oliveira, D. d. A. Honório, L. H. S. Barreto, P. P. Praça, A. Kunzea, and S. Carvalho, "A two-stage AC/DC SST based on modular multilevel converter feasible to ac railway systems," in *Proc. 2014 29th IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1894–1901.
[13] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537–543, Apr. 2002.
[14] A. Huang, "Freedm system-a vision for the future grid," in *Proc. 2010 IEEE Power Energy Gen. Meet.*, 2010, pp. 1–4.
[15] D. Aggeler, J. Biela, and J. Kolar, "Solid-state transformer based on SiC JFETs for future energy distribution systems," in *Proc. Smart Energy Strateg. Conf.*, Zurich, Switzerland, 2008.
[16] K. Mainali *et al.*, "A transformerless intelligent power substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag.*, vol. 2, no. 3, pp. 31–43, Sep. 2015.
[17] L. Heinemann and G. Mauthe, "The universal power electronics based distribution transformer, an unified approach," in *Proc. 2001 IEEE 32nd Annu. Power Electron. Spec. Conf.*, 2001, vol. 2, pp. 504–509.
[18] R. Pena-Alzola, G. Gohil, L. Mathe, M. Liserre, and F. Blaabjerg, "Review of modular power converters solutions for smart transformer in distribution system," in *Proc. 2013 IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 380–387.
[19] X. She, A. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[20] G. De Carne, M. Liserre, and C. Vournas, "On-line load sensitivity identification in LV distribution grids," *IEEE Trans. Power Syst.*, 2016.
[21] G. Buticchi, G. De Carne, D. Barater, Z. Zou, and M. Liserre, "Analysis of the frequency-based control of a master/slave micro-grid," *IET Renew. Power Gener.*, June 2016. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/iet-rpg.2016.0167
[22] X. She, A. Q. Huang, S. Lukic, and M. E. Baran, "On integration of solid-state transformer with zonal dc microgrid," *IEEE Trans. Smart Grid*, vol. 3, no. 2, pp. 975–985, Jun. 2012.
[23] C. Kumar and M. Liserre, "Operation and control of smart transformer for improving performance of medium voltage power distribution system," in *Proc. 2015 IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst.,* Jun. 2015, pp. 1–6.
[24] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage multilevel converters," in *Proc. 2013 IEEE Energy Convers. Congr. Expo.*, 2013, pp. 359–366.
[25] D. Griffel, V. Leitloff, Y. Harmand, and J. Bergeal, "A new deal for safety and quality on MV networks," *IEEE Trans. Power Del.*, vol. 12, no. 4, pp. 1428–1433, Oct. 1997.
[26] A. Cerretti, F. M. Gatta, A. Geri, S. Lauria, M. Maccioni, and G. Valtorta, "Temporary overvoltages due to ground faults in MV networks," in *Proc. IEEE PowerTech*, Jun. 2009, pp. 1–8.
[27] K. Ma, M. Liserre, and F. Blaabjerg, "Operating and loading conditions of a three-level neutral-point-clamped wind power converter under various grid faults," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 520–530, Jan. 2014.
[28] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive power influence on the thermal cycling of multi-MW wind power inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 922–930, Mar. 2013.
[29] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," in *Proc. 2009 IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 3151–3157.
[30] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Rel.*, vol. 42, no. 4, pp. 653–667, 2002.
[31] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. 1997 Int. Conf. Power Electron. Drive Syst.*, 1997, vol. 1, pp. 425–430.
[32] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.
[33] R. Dogan, S. Jazebi, and F. de León, "Investigation of transformer-based solutions for the reduction of inrush and phase-hop currents," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3506–3516, May 2016.
[34] F. Blaabjerg and S. Munk-Nielsen, "Power losses in PWM-VSI inverter using NPT or PT IGBT devices," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 358–367, May 1995.
[35] K. Ma, "Electro-thermal model of power semiconductors dedicated for both case and junction temperature estimation," in *Proc. Power Electron. Next Gener. Wind Turbine Syst.*, Springer, 2015, pp. 139–143.

Markus Andresen (S'15) received the B.Sc. and M.Sc. degrees in electrical engineering and business administration from Christian-Albrechts-University of Kiel, Kiel, Germany, in 2011 and 2012, respectively, where since 2013, he has been working toward the Ph.D. degree in the Chair of Power Electronics.

In 2010, he was an intern in the Delta Shanghai Design Center, Delta Electronics (Shanghai) Co., Ltd., China. His current research interests include control of power converters and reliability in power electronics.

Ke Ma (S'09–M'11) received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2007 and 2010, respectively, and the Ph.D. degree in Power Electronics from Aalborg University, Aalborg, Denmark, in 2013.

In 2013, he was a Postdoctoral fellow in Aalborg University and became an Assistant Professor in 2014. In 2016, he joined the faculty of Shanghai Jiao Tong University, Shanghai, China, as a tenure-track Assistant Professor. His current research interests include the design and enhancement of power electronics reliability in the application of renewable energy and motor drive systems.

Dr. Ma is currently an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and a Guest Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. In 2016, he joined the Thousand Talents Plan Program for Young Professionals, China. He was the receiver of Excellent Young Wind Doctor Award 2014 by the European Academy of Wind Energy, and a few prized paper awards by IEEE.

Giovanni De Carne (S'14) received the Bachelor's and Master's degrees in electrical engineering from Politecnico di Bari, Bari, Italy, in 2011 and 2013, respectively. Since 2013, he has been working toward the Ph.D. degree in power electronics at the University of Kiel, Kiel, Germany.

He is currently working on the "Analysis of ST Features for Electric Distribution Grid" within the European Research Council Grant project, "Highly Reliable and Efficient Smart Transformer-HEART."

Giampaolo Buticchi (S'10–M'13) was born in Parma, Italy, in 1985. He received the Master's degree in electronic engineering in 2009 and the Ph.D. degree in information technologies both from the University of Parma, Parma, Italy, in 2013..

He is currently working as a Postdoctoral Research Associate in the University of Kiel, Kiel, Germany. His research interests include on power electronics for renewable energy systems, smart transformer fed micro-grids, and reliability in power electronics.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) received the Ph.D. degree in Power Electronics from Aalborg University, Aalborg, Denmark, in 1995.

From 1987 to 1988, he was with ABB-Scandia, Randers, Denmark. He became an Assistant Professor in 1992, Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives.

Dr. Blaabjerg has received the 17 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014. From 2006 to 2012, he was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS. He is nominated in 2014 and 2015 by the Thomson Reuters among the most 250 cited researchers in Engineering in the world.

Marco Liserre (S'00–M'02–SM'07–F'13) received the B.Sc. and Ph.D. degree in electrical engineering from the Bari Polytechnic, respectively in 1998 and 2002. He has been Associate Professor at Bari Polytechnic and Professor in reliable power electronics at Aalborg University (Denmark).

He is a Full Professor and the Head of the Chair of Power Electronics at the University of Kiel, Kiel, Germany. He has published more than 200 technical papers (1/3 in international peer-reviewed journals) and a book at second reprint and also translated in Chinese.

Prof. Liserre works have received more than 15 000 citations, for this reason he is listed in ISI Thomson report—The worlds most influential scientific minds from 2014. He has been awarded with the European ERC Consolidator Grant, one of the most prestigious in Europe. He did serve all these societies in various capacities such as Reviewer, Associate Editor, Editor, Conference Chairman, or Track Chairman. He has been the Founding Editor-in-Chief of the IEEE Industrial Electronics Magazine, the Founding Chairman of the Technical Committee on Renewable Energy Systems, and the IES Vice-President responsible of the publications. He has received several IEEE Awards. He is member of IAS, PELS, PES, and IES.